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Mismatch-Shaped Pseudo-Passive Two-Capacitor DAC

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Abstract

A simple mismatch-shaping scheme is proposed for a two-capacitor DAC. Unlike in other mismatch-shaping systems, the shaped error is generated by direct filtering of a well-defined bounded signal, which can be generated as white noise. The operation is closely related to a specific digital interpolation filter, but arbitrary properties of the overall interpolation characteristic can be assured.

Simulations indicate that the scheme can be used for the realization of DACs with 16-bit linearity and SNR performance, with only 0.1% capacitance accuracy. The DAC is pseudo-passive, i.e. an active element is required only to buffer the output signal. Hence, it is potentially a very low-power circuit, suitable for portable applications.

1: Introduction

High-performance digital-to-analog converters (DACs) are required for a variety of portable applications, e.g. audio equipment. The signal-to-noise-and-distortion ratio (SNDR) is often required to be as large as 90–100dB; a level of performance which cannot be obtained by brute-force implementation of DACs which rely on accurate matching of electrical parameters.

Error-shaping DACs have become popular, because they facilitate inherently-linear D/A conversion despite the mismatch of electrical parameters. In this way, expensive laser trimming and elaborate background-calibration techniques can be avoided.

Portable equipment requires the power consumption be low, which conflicts somewhat with single-bit delta-sigma DACs' requirement for high-performance switched-capacitor (SC) filters [1] [2].

Fig. 1 shows the implementation of a DAC system, with special emphasis on the analog reconstruction filter. The key points include the following two:

1. The opamp's output is controlled by passive charge sharing between C_1 and C_f , and it need drive only the load posed by the low-pass filter. Thus, the opamp can be designed to have a much lower power consumption than if it would have to recharge C_f in every sample (cf. [2]).
2. The opamp's output is evaluated as a continuous-time (CT) signal, and hence the SC stage performs the DAC's discrete-time to continuous-time (DT/CT) conversion. This implies that the opamp's input-referred noise is not subject to aliasing, but also that the stage is sensitive to clock jitter [3].

To avoid clock-jitter-induced limitations, and to facilitate linear DT/CT conversion, it is imperative that the DAC provides a multi-level output signal $y(n)$ [3]. Instead of (as usual) employing a delta-sigma modulator, a switched-capacitor filter [4] and/or a unit-element mismatch-shaping DAC [5], this paper will consider the simplest possible option, which is to use only the capacitor C_1 , a voltage reference V_{ref} , and a few switches to implement a pseudo-passive DAC [6]. The very low power consumption, low circuit complexity, and full compatibility with CMOS technology are among the many advantages associated with this approach. The achievable bandwidth is relatively low, but it is wide enough for audio applications, and by employing a few circuit tricks, it may extend into the low MHz range.

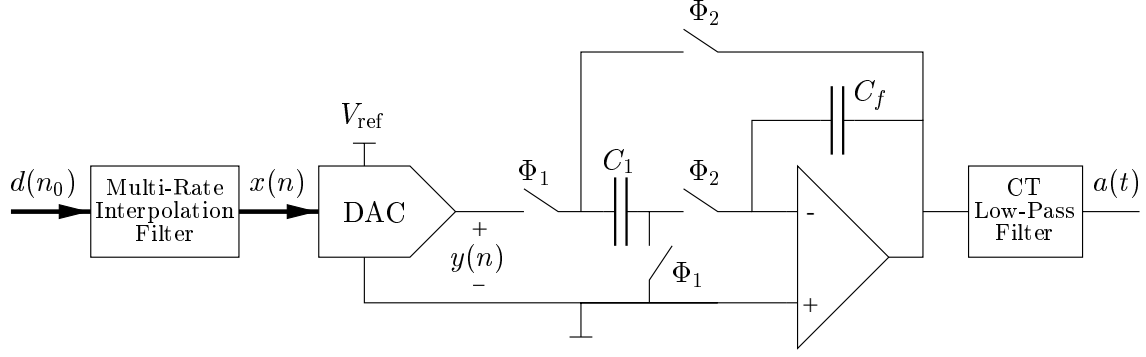


Figure 1. Overall D/A converter system.

2: Pseudo-passive two-capacitor DAC

Suarez et al. [6] proposed the very economical DAC shown in Fig. 2, where the clock phases Φ_1 and Φ_2 are the same as in Fig. 1, and where C_1 is separated into C_{11} and C_{12} of the same nominal value. It functions by first discharging the two capacitors, followed by a sequence of N cycles ($k \in \{1, 2, \dots, N\}$, where N is the resolution of $x(n)$), in which C_{11} is first (in clock phases Φ_1) charged to 0 or V_{ref} according to $x(n, k)$ (the k th bit of $x(n)$) where after (in clock phases Φ_2) C_{11} and C_{12} are connected in parallel to facilitate charge sharing.

The bit signal $x(n, k)$ operates at the fast clock frequency f_a , and it takes $N + 1$ cycles to D/A convert a sample $x(n)$. Thus, the sampling frequency (with respect to n) is $f_s[n] = f_a/(N + 1)$. As for most DACs, its linearity depends on the matching of electrical parameters – in this case the matching of C_{11} and C_{12} . After an initial analysis, some techniques to improve the linearity will be discussed.

2.1: Analysis of the pseudo-passive two-capacitor DAC

Define $v(n, k)$ as the voltage across C_1 in the k th clock phase Φ_b . Each D/A conversion is initiated by a reset phase Φ_{reset} , thus $v(n, 0) = 0$ for all n .

Just before the k th clock phase Φ_b , capacitor C_{12} will have the voltage $v(n, k - 1)$, and capacitor C_{11} will have the voltage $x(n, k)V_{\text{ref}}$. During clock phase Φ_b , charge sharing yields the following relation

$$v(n, k) = \frac{C_{11}}{C_{11} + C_{12}} x(n, k)V_{\text{ref}} + \frac{C_{12}}{C_{11} + C_{12}} v(n, k - 1) \quad (1)$$

By introducing the mismatch parameter

$$\delta = \frac{C_{11} - C_{12}}{C_{11} + C_{12}} \quad (2)$$

Eqn. (1) can be brought to the form

$$\begin{aligned} v(n, k) &= \frac{1 + \delta}{2} x(n, k)V_{\text{ref}} + \frac{1 - \delta}{2} v(n, k - 1) \\ &= \frac{x(n, k)V_{\text{ref}} + v(n, k - 1)}{2} + \frac{\delta}{2} [x(n, k)V_{\text{ref}} - v(n, k - 1)] \end{aligned} \quad (3)$$

The first term in Eqn. (3) represents the ideal operation

$$y_{\text{ideal}}(n) = v_{\text{ideal}}(n, N) = \frac{V_{\text{ref}}}{2} \sum_{k=1}^N x(n, k)2^{k-N} = \frac{V_{\text{ref}}}{2} x(n) \quad (4)$$

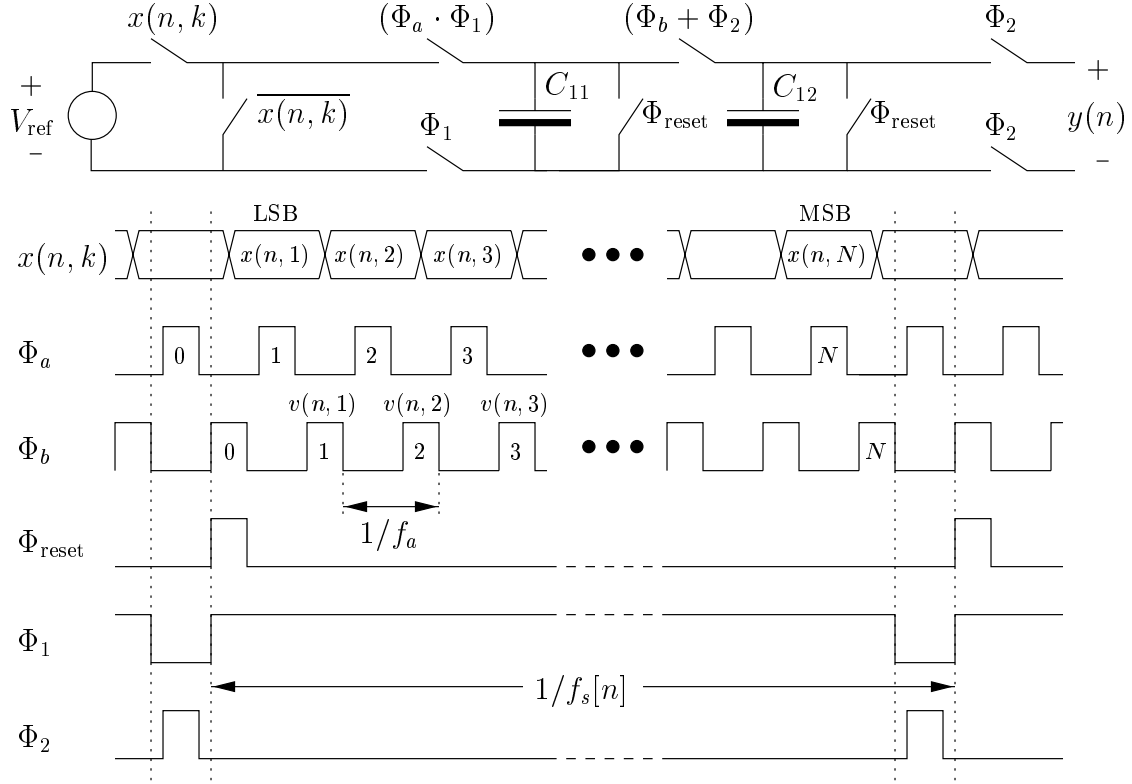


Figure 2. Pseudo-passive two-capacitor DAC based on the charge-sharing principle.

whereas the second term represents the error caused by capacitor mismatch. For all practical purposes, it is sufficient to consider only the first-order errors (i.e. the terms that have a coefficient δ^p , where $p \geq 2$, may be neglected), and hence $\delta v(n, k-1)$ can be approximated by $\delta V_{\text{ref}} \sum_{j=1}^{k-1} x(n, j) 2^{j-k}$. This leads to the following evaluation of the error signal

$$e(n) = y(n) - y_{\text{ideal}}(n) = \delta \frac{V_{\text{ref}}}{2} \sum_{k=1}^N \left[x(n, k) - \sum_{j=1}^{k-1} x(n, j) 2^{j-k} \right] 2^{k-N} \quad (5)$$

Notice that the sum in Eqn. (5) is a function of only $x(n, k)$, i.e. the error signal can be considered to be of the form $e(n) = \delta V_{\text{ref}} F[x(n, k)]$.

By combining Eqn. (3) and (5), it follows that the total harmonic distortion (THD) in principle can be calculated analytically except for the unknown parameter δ , to which the THD is proportional. Because an analytical expression will not provide any valuable insight, the THD performance was evaluated only on the basis of simulation. It was found that, for a full-scale sinusoid input, the THD is approximately $(-5 + 20 \log_{10}(\delta))$ dB. Unfortunately, even when using the best known layout techniques, δ cannot be made much smaller than 0.1%, corresponding to only about 11-bit linearity.

2.2: Charge injection and clock feedthrough

An important feature of the two-capacitor DAC is that symmetry makes it insensitive to clock feedthrough and charge injection (charge errors).

Consider first the behavior in clock phases Φ_a , where capacitor C_{11} is charged to either 0 or V_{ref} . Indeed, when the switch controlled by Φ_a is opened, charge errors will cause a change in the voltage

stored on C_{11} . The charge error will in general be a nonlinear function of the switch's potential, but because the capacitor is charged to one of only two values, the charge error can be modeled as a linear error. In other words, although C_{11} may not be charged to exactly $0/V_{\text{ref}}$, it will be charged to one of two time-invariant values, and hence the error can be modeled as an offset and a gain error.

Now consider the behavior in clock phases Φ_b , where the charge on capacitors C_{11} and C_{12} is shared. Considering that the top plates of the two capacitors constitute an electrically isolated system, it follows that the charge which is trapped in the conductive switch's channel must originate from within the isolated system (i.e. from the capacitors' top plates). When the switch is turned off, the channel charge will find its way back to the capacitors. The decisive point is that – providing good electrical symmetry – equal amounts of charge will flow to the two capacitors, and hence the total charge will be shared equally despite charge injection. Notice that it is important to assure good symmetry of the layout, and not to turn the switch off too abruptly to prevent charge being pumped into the substrate (a nonlinear effect). Using a similar argumentation, it can be shown that the charge-sharing operation also is insensitive to clock feedthrough.

3: Compensative switching

Compensative switching schemes can be used to improve the DAC's linearity. The fundamental idea, proposed in [7], is that C_{11} and C_{12} can be interchanged at any time when the two capacitors are connected in parallel (cf. Fig. 2). In the following, $t(n, k) = 1$ will denote that C_{11} is charged in the k th clock phase Φ_a of the n th sample, whereas $t(n, k) = -1$ denotes that C_{12} is charged instead (i.e. that the capacitors are interchanged). The error signal $e(n)$ can then be represented in the form (cf. [8])

$$e(n) = y(n) - y_{\text{ideal}}(n) = \delta \frac{V_{\text{ref}}}{2} \sum_{k=1}^N t(n, k) \left[x(n, k) - \sum_{j=1}^{k-1} x(n, j) 2^{j-k} \right] 2^{k-N} \quad (6)$$

3.1: Error-canceling switching

In [9], it is shown that it is not possible to choose $t(n, k)$ such that $e(n) = 0$ for all $x(n)$, but by performing two D/A conversions and adding the results in the analog domain, it is actually possible to cancel the error $e(n)$. The method proposed in [9] requires the use of complex digital circuitry, but fortunately the same performance can be obtained using a much simpler technique.

By identifying that the polarity of $e(n)$ can be alternated simply by inverting $t(n, k)$ for all k , it follows that an ideal D/A conversion $y(n) = V_{\text{ref}}x(n)$ can be obtained by D/A converting $x(n)$ twice (with opposite but arbitrary values of $t(n, k)$) and adding the two resulting voltages. A passive technique can be used to implement the summation. After each of the two conversions, $C_{11} + C_{12}$ is connected in parallel with one of two previously discharged capacitors (say) C_{31} and C_{32} of the same nominal value. By afterwards connecting C_{31} and C_{32} in parallel, the resultant voltage will (to a first-order approximation) be proportional to $V_{\text{ref}}x(n)$, and hence $C_{31} + C_{32}$ can be used in the place of C_1 in Fig. 1.

Although this technique is both useful and simple, it should be understood that it also has some disadvantages. Besides the requirement for extra hardware (the capacitors C_{31} and C_{32}), the frequency of the fast clock f_a must be doubled, and hence the bandwidth/power ratio will be cut in half. Also, the thermal-noise characteristics are degraded, which requires the use of larger capacitors, whereby the power consumption is further increased.

3.2: Mismatch-shaping switching

Now referring to Fig. 1, it should be understood that $y(n)$ must be somewhat oversampled (i.e. the sampling frequency f_s must be a factor of OSR higher than twice the maximum signal-band

frequency f_b) no matter how the DAC is implemented. This is a requirement, because it is difficult to implement a CT analog low-pass filter which efficiently can suppress the signal band's spectral replica images, unless the OSR is at least in the order of 10–30. In fact, to minimize the power consumption, the CT low-pass filter should be as simple as possible, and preferably implemented as a passive circuit (or on the basis of the same opamp).

Considering that $e(n)$ will represent only very little power (typically less than -60 dBFS), it may be understood that it is not necessary to actually cancel it, as long as it can be assured that it does not corrupt the signal-band performance. Indeed, it is possible to convert each sample $x(n)$ only once (i.e. using only as many clock cycles as the resolution of $x(n)$), by choosing $t(n, k)$ such that $e(n)$ has only very little power in the signal-band. This very general (and fairly simple) approach was suggested in [8], where it was shown that $e(n)$ can be made negligible even if the OSR is as low as 10. Because the DAC system requires at least this degree of oversampling to simplify the analog reconstruction filter, it follows that mismatch-shaping DACs in general are preferable (compared to error-canceling DACs), because the fast clock f_a (which is proportional to the power consumption) will be reduced by a factor of two.

The following will show that the mismatch-shaping property can be obtained using a technique which is even simpler than that proposed in [8]. The advantages include a simplification of the layout, and a reduction in the power consumption. The concept relies on the integration of the DAC with the digital interpolation filter, and typically also with the analog reconstruction filter.

3.2.1: First-order mismatch-shaping switching

The digital interpolation filter will in general be implemented as a cascade of filter stages (cf. Fig. 3). The requirements to the first filter stage are typically rather strict (narrow transition band and efficient suppression of the first spectral replica image), whereas the following stages may be simpler. In the following, it will be assumed that the last stage is implemented as a simple zero-order holding filter, which increases the sampling frequency by repeating the same sample.

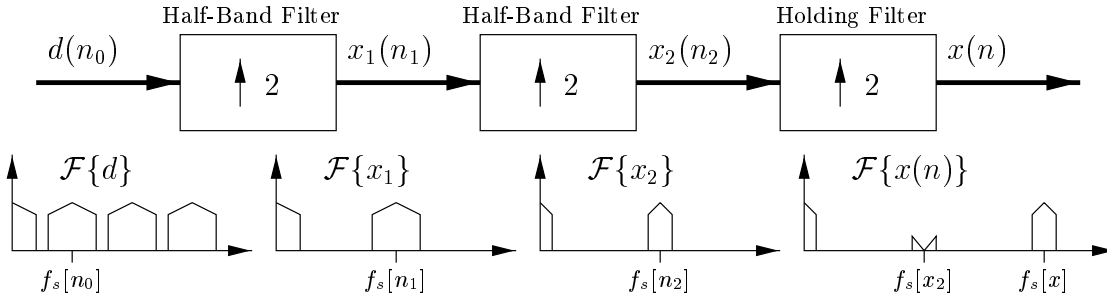


Figure 3. Typical implementation of an interpolation filter

Assuming that the last stage of the interpolation filter is a frequency-doubling zero-order holding filter, it follows that $x(n)$ will be a sequence of pairs, i.e.

$$x(n) = \dots, \underset{\text{<same value>}}{x_2(q), x_2(q)}, \underset{\text{<— same value —>}}{x_2(q+1), x_2(q+1)}, \underset{\text{<— same value —>}}{x_2(q+2), x_2(q+2)}, \dots \quad (7)$$

If C_{11} and C_{12} are interchanged in the two conversions of each value $x_2(n_2)$, it follows that the error signal will be of the form

$$e(n) = \dots, \underset{\text{<sequence>}}{e_q, -e_q}, \underset{\text{<sequence>}}{e_{q+1}, -e_{q+1}}, \underset{\text{<sequence>}}{e_{q+2}, -e_{q+2}}, \dots \quad (8)$$

which can be interpreted as the first-order difference of

$$e^*(n) = \dots, e_q, 0, e_{q+1}, 0, e_{q+2}, 0, \dots \quad (9)$$

The signal $e^*(n)$ can be considered to be generated by the same DAC system for the situation where the last stage of the interpolation filter increases the sampling frequency by inserting zeroes rather than holding the value. Hence, for $t(n, k) = 1$, $e^*(n)$ will include *harmonic distortion* of $d(n_0)$. Considering that $e(n) = e^*(n) - e^*(n-1)$, it follows that the in-band harmonic distortion included in $e(n)$ is suppressed by 20 dB for every decade of oversampling. In other words, for OSR=10 and a 0.1% relative matching of C_{11} and C_{12} , the worst-case in-band THD performance will be in the order of -85 dB, rather than just -65 dB.

As always for mismatch-shaping systems, it is preferable if the power of $e^*(n)$ is equally distributed over all frequencies (i.e. that $e^*(n)$ is white noise), rather than concentrated at discrete frequencies. Because the first sample of each pair of samples in Eqn. (7) may be D/A converted using either C_{11} or C_{12} as the driving capacitor (as long as the capacitors are interchanged in the D/A conversion of the other sample), $e^*(n)$ need not be a tonal signal. Tonality can be perfectly prevented by *randomly* choosing which capacitor to use first. This mode of operation can be described as

$$t(n, k) = \begin{cases} \text{random}\{-1, 1\} & \text{for } n \text{ even} \\ -t(n-1, k) & \text{for } n \text{ odd} \end{cases} \quad (10)$$

Although it is not a requirement, the simplest implementation is of course to let $t(n, k)$ be independent of k , in which case only one random bit has to be generated for every other sample $x(n)$. A study will show that the random generator need not have very good stochastic properties.

3.2.2: Higher-order mismatch shaping

Usually it is not necessary, but if the relative matching δ of the two capacitors is poor, higher-order mismatch shaping may be an option worth pursuing.

To achieve second-order mismatch-shaping, the last interpolation stage should increase the sampling frequency by a factor three, and the goal is to make the error signal of the form

$$e(n) = \dots, \quad e_q, -2e_q, e_q, \quad e_{q+1}, -2e_{q+1}, e_{q+1}, \quad e_{q+2}, -2e_{q+2}, e_{q+2}, \quad \dots \quad (11)$$

<- sequence -> <- - sequence - -> <- - sequence - ->

The simplest way to scale the errors is to scale the output $y(n)$ in the analog domain. Because amplification cannot be implemented passively, the first and the third sample of each sequence should instead be scaled by a factor 0.5, e.g. using a capacitive voltage divider. This operation can be implemented in many ways, the simplest is possibly to use the available analog hardware and make a small modification of the digital control signals

$$x(n) = \begin{cases} 0.5x_2(n/3) & \text{for } \text{modulo}(n, 3) = 0 \\ x_2((n-1)/3) & \text{for } \text{modulo}(n, 3) = 1 \\ 0.5x_2((n-2)/3) & \text{for } \text{modulo}(n, 3) = 2 \end{cases} \quad (12)$$

$$t(n, k) = \begin{cases} \text{random}\{-1, 1\} & \text{for } \text{modulo}(n, 3) = 0 \text{ and } k \neq N \\ 1 & \text{for } \text{modulo}(n, 3) = 0 \text{ and } k = N \\ -t(n-1, k-1) & \text{for } \text{modulo}(n, 3) = 1 \\ t(n-2, k) & \text{for } \text{modulo}(n, 3) = 2 \end{cases} \quad (13)$$

The second entry line in Eqn. 13 is very important, because it assures the the scaling coefficient $\frac{C_{12}}{C_{11}+C_{12}} \simeq 0.5$ is time-invariant, and hence that capacitor mismatch will not cause nonlinearity, but only a negligible uncertainty of the transfer function by which the noise signal $e^*(n)$ is shaped.

The interpolation described by Eqn. (12) does not reject the spectral replica images of $x_2(n_2)$ efficiently. However, as described in the next section, a simple modification of the system can provide almost arbitrarily good rejection of undesired spectral components, and hence this minor disadvantage is not a real limitation.

Clearly, arbitrary mismatch-shaping transfer functions can be obtained in a similar way.

4: Interpolation in the analog domain

A CT analog filter (cf. Fig. 1) may be used to suppress unwanted spectral replica images, but because this filter must honor the overall system performance, the hardware penalty may be significant.

Considering that the two-capacitor DAC (including the required digital control circuitry) is so simple that multiple replicas easily can be implemented on a very small chip area, it may actually be simpler to implement a discrete-time analog FIR filter as shown in Fig. 4. It can be considered to be a generalization of Fig. 1, where C_1 is separated in multiple capacitors $a_i C_1$ which are charged individually in clock phases Φ_1 and connected in parallel with C_f in clock phases Φ_2 . Each DAC and the corresponding capacitor $a_i C_1$ in combination represent a two-capacitor DAC of the type shown in Fig. 2.

The total capacitance $C_1 = \sum_i a_i C_1$ is determined mainly by the required thermal-noise performance. Because the power consumption largely is proportional to $f_a C_1$, it may be understood that the implementation of the proposed FIR filter will have an only very small impact on the overall power consumption.

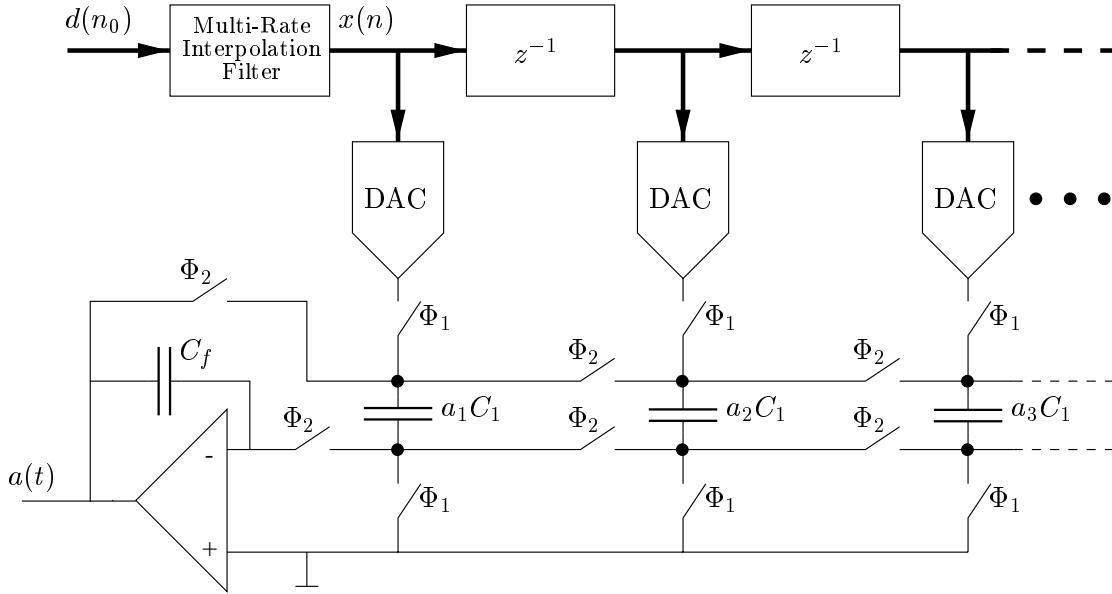


Figure 4. Reconstruction filter including an analog FIR filter.

The FIR filter's transfer function can be calculated as $H_{\text{FIR}}(z) = \sum_i a_i z^{1-i}$, and good suppression of spectral replica images can be obtained by proper choice of the coefficients a_i (minor modifications are required to implement negative coefficients).

In principle, it is possible to implement the overall digital interpolation filter as a simple zero-order holding filter, but this will not be an optimal design, because the FIR filter then will have to be very long. On the other hand, designing the FIR filter with only one tap (cf. Fig. 1) is not optimum either, because the holding characteristic of the interpolation filter's last stage will in general not provide sufficient suppression of the spectral replica images centered around $qf_s[n_2]$. Thus, good designs will use DSP to allow the FIR filter to have a fairly wide transition band, such that it can be implemented with only (say) 2–10 taps. The use of an analog FIR filter is especially relevant when the D/A converter is designed to be second-order mismatch-shaping, because in that case the last-stage interpolation provides only little suppression of the relevant spectral replica images.

To optimize the bandwidth/power ratio, it is preferable if $x(n)$ is not oversampled too much. However, to avoid the need for a CT analog filter, C_f should be updated at a high frequency (to

minimize the step size in $a(t)$). These conflicting requirements can be fulfilled simultaneously only if the analog reconstruction filter is designed as a multi-rate filter, i.e. by performing interpolation in the analog domain.

The analog FIR filter can be implemented as a multi-rate filter by connecting several (say three) DACs to each node between the delay elements (cf. Fig. 4), and by controlling them with (three) sets of clock signal $(\Phi_1, \Phi_2), (\Phi_1', \Phi_2'), (\Phi_1'', \Phi_2'')$, which are skewed one (third) of a sampling period relative to each other. Once again, it should be understood that the total capacitance is the dominant factor for both the power consumption and the thermal-noise performance, and hence that the power consumption need not be affected significantly by the implementation of the analog filter.

Notice that, if the interpolation is implemented mainly in the analog domain, $x(n)$ may be oversampled too little to make use of mismatch-shaping DACs, in which case error-canceling DACs will have to be used instead.

Finally, notice that the bandwidth/power ratio also can be improved by reducing the resolution of $x(n)$ to (say) 8–10 bits before the D/A conversion. A multi-bit delta-sigma modulator is required for this purpose.

5: Simulation results

A second-order mismatch-shaping DAC system has been simulated. $x_2(n_2)$ (cf. Fig. 3) was assumed 4 times oversampled and was modeled as a sinusoid at the highest signal-band frequency. To facilitate second-order mismatch shaping, $x(n)$ had to be oversampled three times higher, i.e. 12 times. The analog signal was filtered by a 5-tap FIR filter with the coefficients 0.12, 0.22, 0.32, 0.22, 0.12.

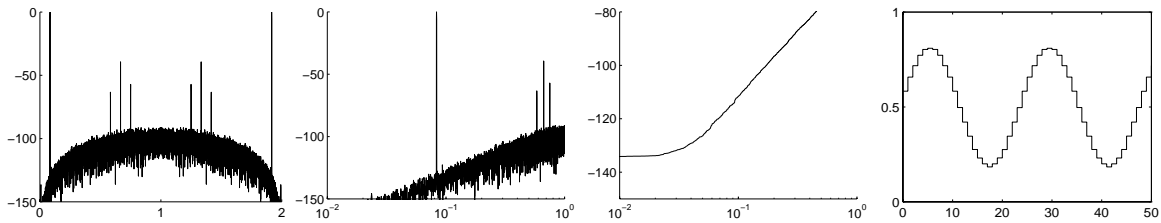


Figure 5. Simulation results for a second-order mismatch-shaping DAC system

Fig. 5 shows the simulation result for the situation where $\delta = 0.1\%$. The two plots to the left show the FFT (in dB) of $y(n)$ (the holding characteristic of the DT/CT conversion is not included) versus the frequency normalized with respect to the Nyquist frequency $f_s/2$. The mismatch-shaping property is evident. Notice that the three-tone clusters are *not* idle tones, but spectral replica images of the signal band (which includes a dc component). The third plot from the left shows the signal-band SNDR (in dBFS) versus the highest signal-band frequency (i.e. $1/\text{OSR}$). A 100 dB SNDR is obtained at only 6 times oversampling, which indicates that first-order mismatch shaping will be sufficient for most purposes. The saturation at approx. -135 dBFS is caused by the second-order capacitor-mismatch errors, which were neglected in the above discussion. The waveform of $y(n)$ is shown to the right, which indicates that a fairly simple analog filter will be sufficient to smoothen the signal.

6: Conclusion

A low-power D/A converter system based on pseudo-passive techniques has been proposed. The core of the system is a simple two-capacitor serial DAC, for which nonlinearity is prevented by

using a novel mismatch-shaping technique. Unlike other mismatch-shaping techniques, the system is inherently stable, and idle tones are effectively avoided.

Each input sample is D/A converted P times, and the sequence of outputs is scaled in the analog domain. The signal and the corresponding error can be modeled as the output of two FIR filters of length P and with coefficients of the same magnitude (the P scaling factors). The fundamental idea in the mismatch-shaping scheme exploits that the error's polarity can be altered, and hence that the polarity of the two FIR filters' coefficients need not be the same. In essence, the challenge is to design the two FIR filters, $H_{\text{pass}}(z)$ and $H_{\text{stop}}(z)$, such that the frequency response of $H_{\text{pass}}(z)$ is relatively flat in the signal band, and such that $H_{\text{stop}}(z)$ suppresses signal-band spectral components. Short FIR filters with good properties of $H_{\text{stop}}(z)$ will in general be preferred, because the signal transfer function easily can be adjusted using other means.

The two-capacitor DAC's serial operation combined with the requirement for P conversions of each sample will potentially limit the bandwidth somewhat. To prevent this scenario, an analog interpolation technique has been proposed. The technique exploits the extreme simplicity of the proposed mismatch-shaping scheme, which facilitates a compact and modular implementation of the many required DACs.

The DAC system can be designed to have a very low dc power consumption, and simulations indicate that it can provide very high resolution at a low oversampling ratio. Hence it is very suitable for use in portable equipment.

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